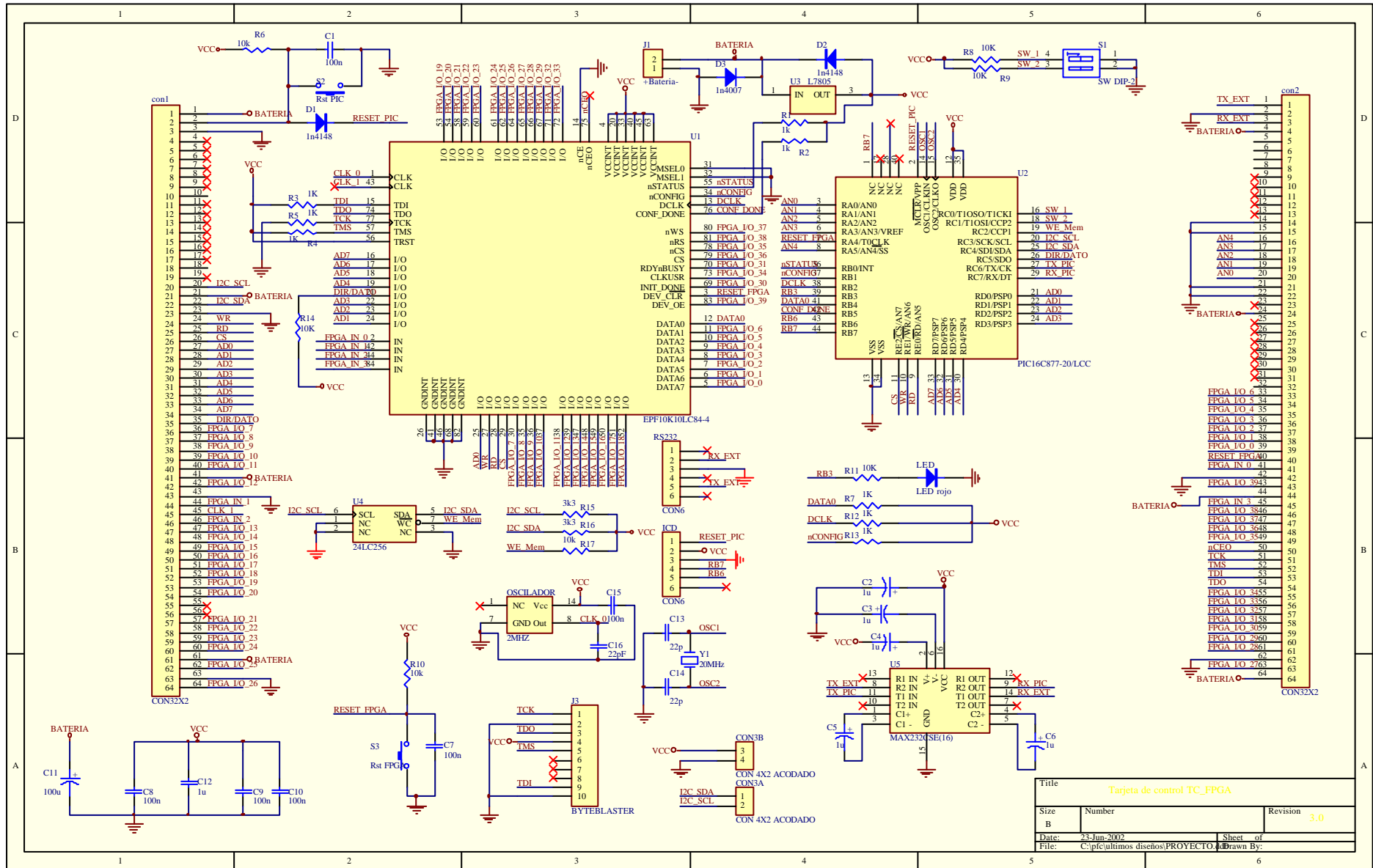
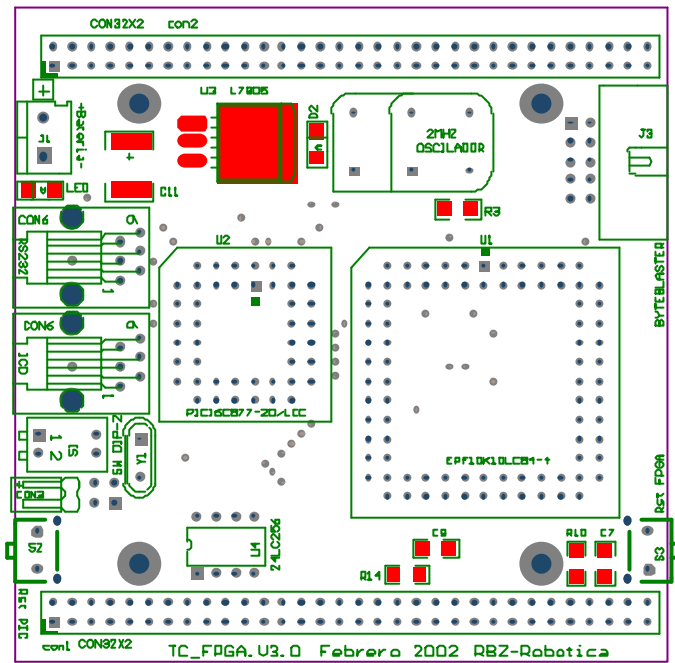


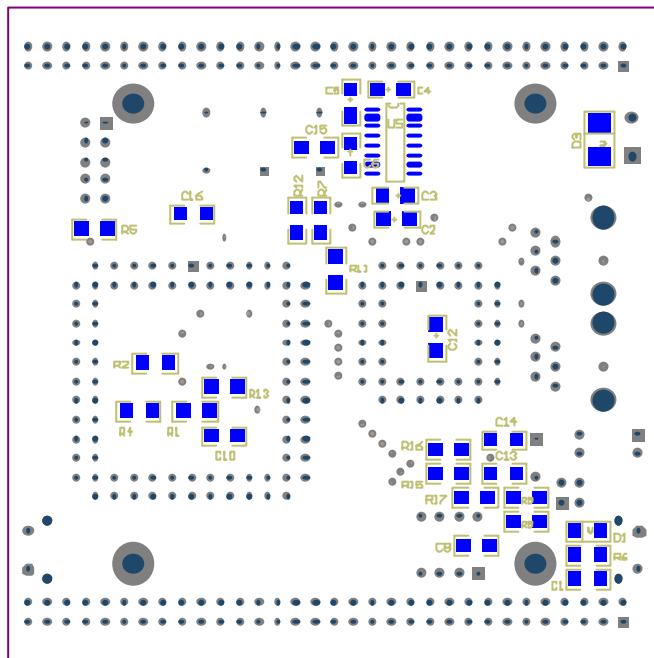
II. PLANOS:



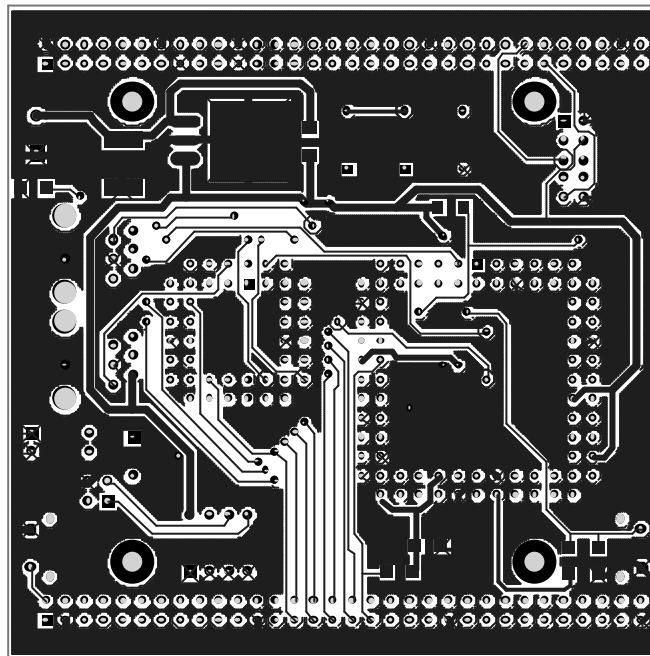
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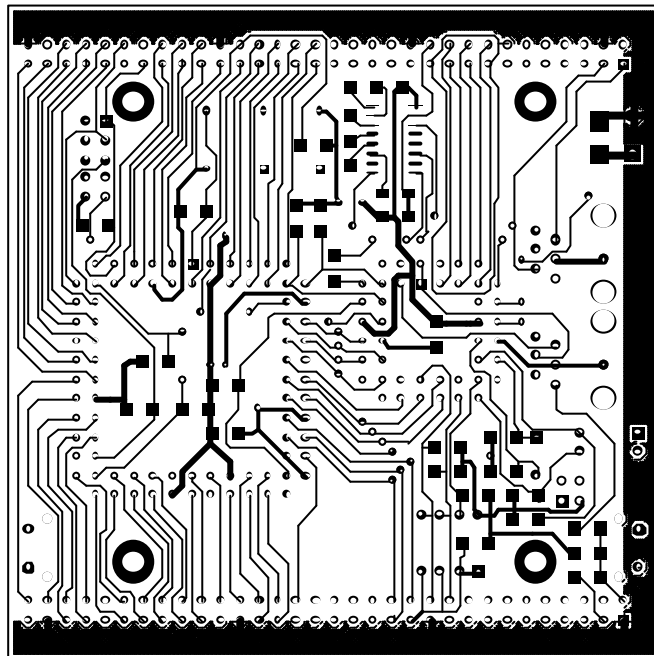
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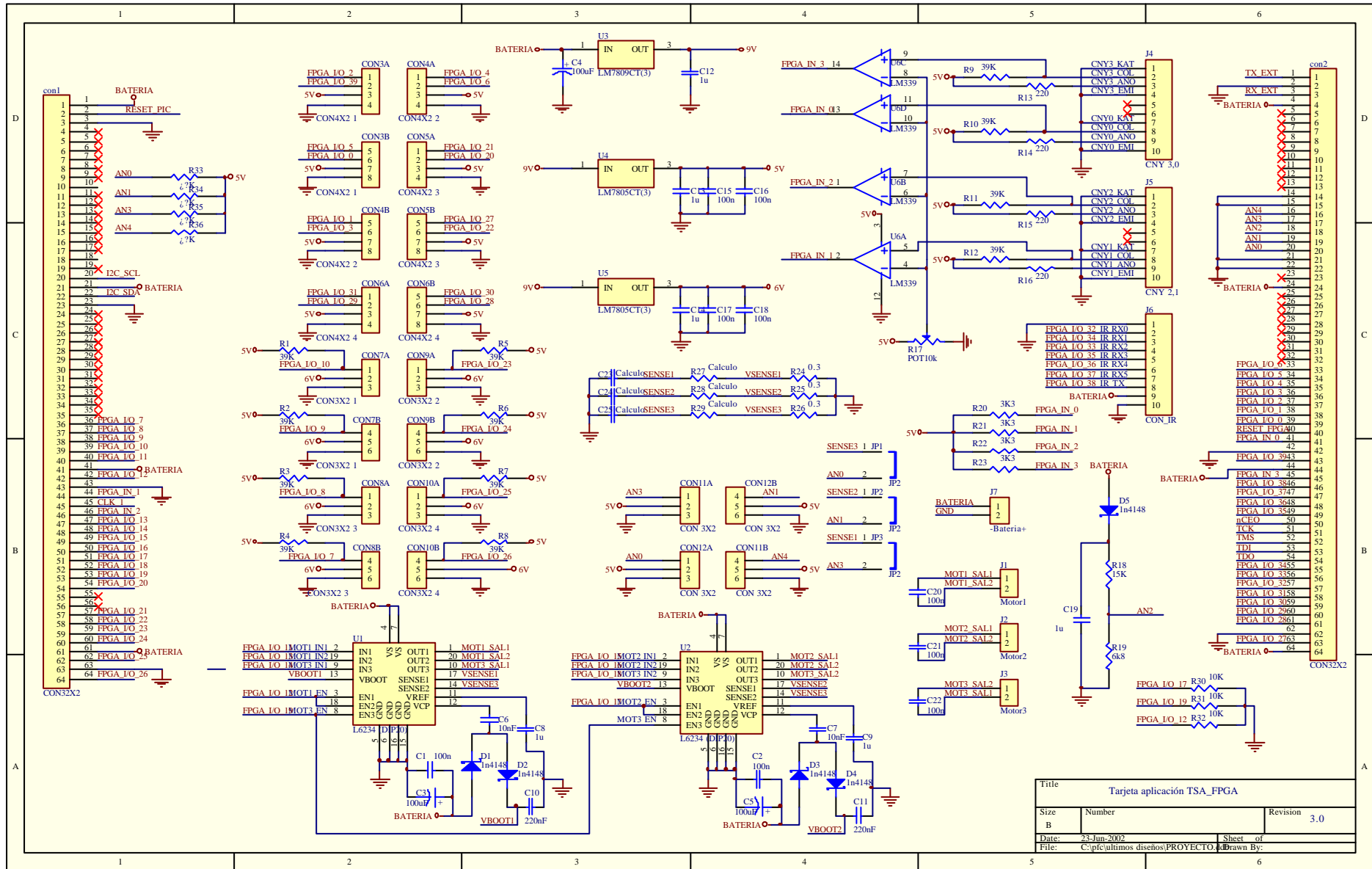
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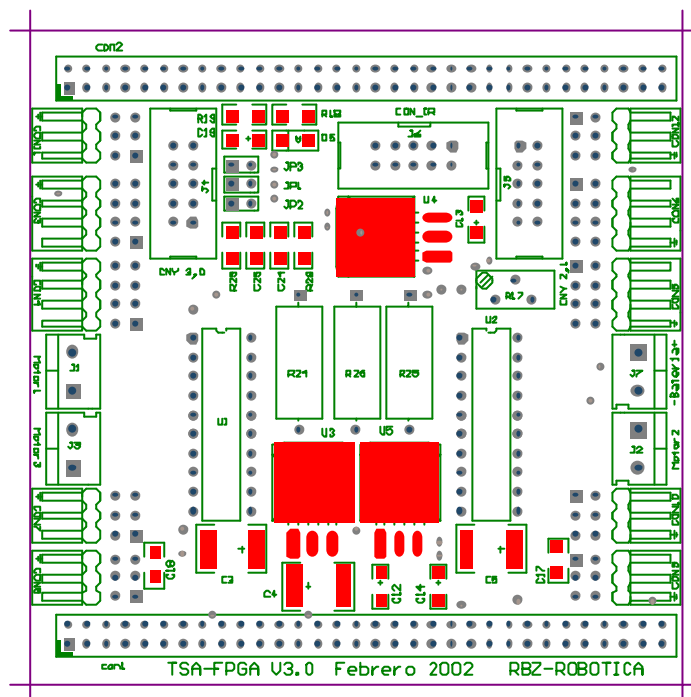
Pistas top, TC_FPGA



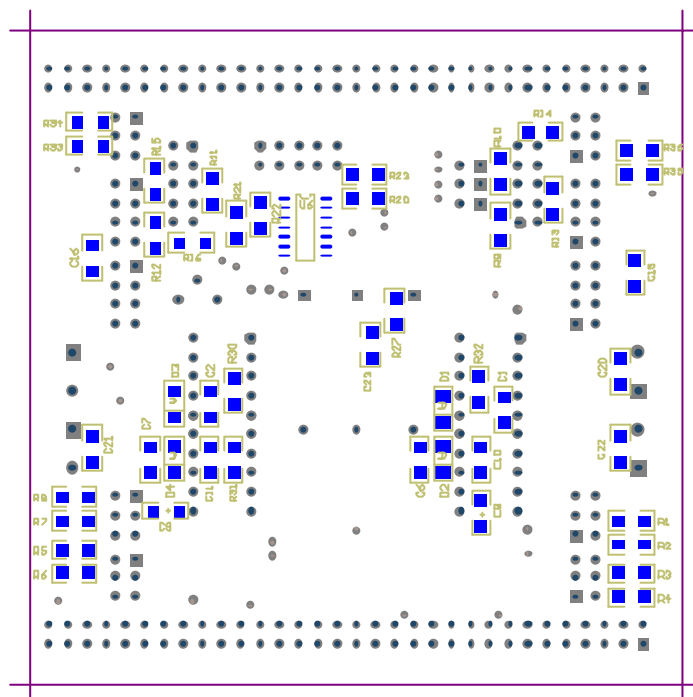
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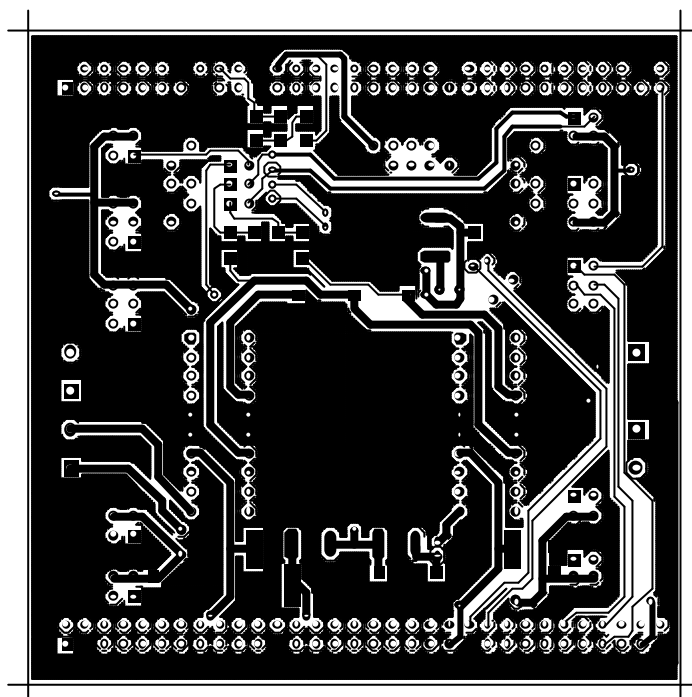
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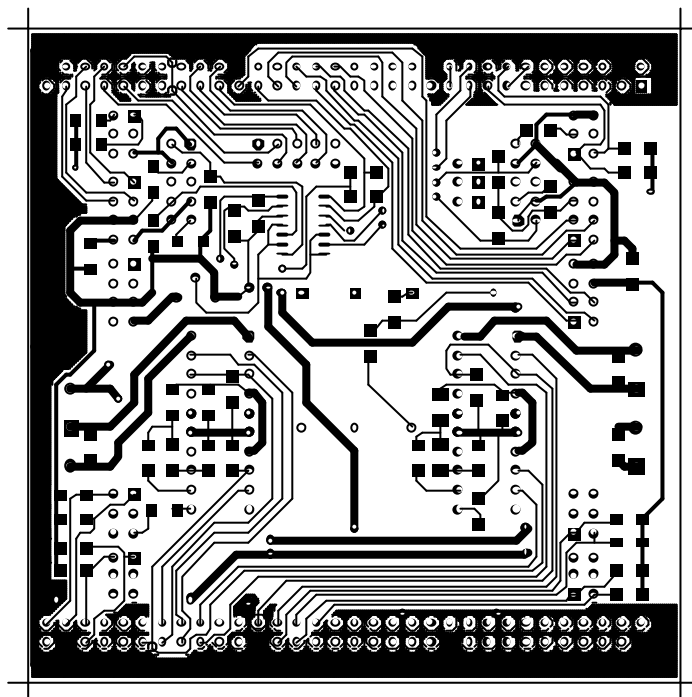
Serigrafia Top, TSA_FPGA



Serigrafia bottom, TSA_FPGA



Pistas TOP, TSA_FPGA



Pistas bottom, TSA_FPGA

